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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,086	02/17/2004	Brock J. LaMeres	10031039-1	3393

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EXAMINER	
HOLLINGTON, JERMELE M	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 04/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/781,086	Applicant(s) LAMERES ET AL.	
	Examiner Jermele M. Hollington	Art Unit 2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20 and 21* is/are allowed.

6)☒ Claim(s) *1-9 and 22-25* is/are rejected.

7)☒ Claim(s) *10-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: on page 1, paragraph [0002], line 4, after "2003" and before ")" add the following --now U.S. Patent No. 6,867,609--, and on line 7 in the same paragraph after "2003" and before ")" add the following --now U.S. Patent No. 6,822,466--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 4, and 6-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Schmid et al.(6150830).

Regarding claim 1, Schmid et al disclose [see Fig. 2] a probe (test head 1) for probing test points (test points 3) on a target board (electric component under test 5, comprising: a first printed circuit board (PCB) (connecting element 11) having a plurality of signal routes (line 35) for routing signals to a test instrument [not shown]; and a plurality of spring pins (contact elements 25) for probing the test points (3) on the target board (5), each spring pin (25) of which is i) disposed perpendicularly to the first PCB (11), and ii) electrically coupled [via contact point 31] to at least one signal route (35) of the first PCB (11).

Regarding claim 2, Schmid disclose the first PCB (11) has a plurality of holes (holes 37) that frictionally engage bodies of at least some of the plurality of spring pins (25).

Regarding claim 4, Schmid et al disclose said signal routes (35) comprise tip-network components positioned adjacent said spring pins (25).

Regarding claim 6, Schmid et al disclose an alignment mechanism (combination of screws 9 and base body 13), attached to the first PCB (11), for aligning the probe (1) with respect to said test points (3).

Regarding claim 7, Schmid et al disclose the alignment mechanism (9 with 13) comprises a plurality of alignment pins (screws 9).

Regarding claim 8, Schmid et al disclose comprising a mechanism (screws 9), attached to the first PCB (11), for securing the probe (1) to said target board (5).

Regarding claim 9, Schmid et al disclose said mechanism (9) is a plurality of rivets (screws 9).

4. Claims 22-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Murphy (5157325).

Regarding claim 22, Murphy discloses probing test points (test contact points 16) on a target board (printed circuit board under test 14), comprising: selecting a test probe (fixture 20) comprising a plurality of spring pins (test pins 30) that are arranged perpendicularly to a main body (PCB 26) portion of the test probe (20), said main body portion (26) comprising a first printed circuit board (PCB) to which the plurality of spring pins (30) are electrically coupled [via test contact points 38); moving the test probe (20) over the target board (14) to seat an alignment mechanism (screws 36) of the test probe (20) to a corresponding alignment mechanism (36) of

the target board (14); applying pressure [see arrow 64 and 98] to at least one of the i) test probe (20) or ii) target board (14) to cause the plurality of spring pins (30) to engage the test points (16) on the target board (14); and routing signals from the test points (16) to a test instrument via the test probe (20).

Regarding claim 23, Murphy discloses while applying said pressure [shown as arrows 64 and 98], applying enough pressure to cause a securing mechanism of the test probe (20) to engage a securing mechanism of the target board (14).

Regarding claim 24, Murphy discloses said moving comprises moving said first PCB (26) along a path that is substantially parallel to said target board (14).

Regarding claim 25,Murphy discloses the spring pins (30) of the selected test probe (20) are electrically coupled to traces (32) of a second PCB (PCB 28) that is perpendicularly attached to the first PCB [via connector 88 and 94].

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schmid et al (6150830) in view of Holcombe et al (6867609).

Regarding claim 3, Schmid et al disclose [see Fig. 2] the first PCB (connecting element 11) has a plurality of plated holes (holes 37), each of which is electrically coupled to at least one signal route (line 35) of the first PCB (11); and at least some of the spring pins (contact elements 25). However, they do not disclose the spring pins are inserted into and soldered to the plated holes as claimed. Holcombe et al disclose a first PCB (support 210) with a least one-signal route (coaxial cable 260) and spring pins (spring pins 230) are inserted into and soldered to the plated holes [see col. 3, lines 19-62]. Further, Holcombe et al teach that the addition of spring pins inserted into and soldered to the plated holes is advantageous because it provides impedance matching, or equivalent load matching, thereby reducing the electrical intrusiveness of the probe on the target board. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Schmid by adding spring pins inserted into and soldered to the plated holes as taught by Holcombe et al in order to provide impedance matching, or equivalent load matching, thereby reducing the electrical intrusiveness of the probe on the target board.

Regarding claim 5, Schmid et al disclose said tip-network components (part of line 35). However they do not disclose tip-network components comprise isolation resistors as claimed. Holcombe et al disclose tip-network component (220a) comprise isolation resistors [see col. 3, lines 33-34 and lines 42-44]. Further, Holcombe et al teach that the addition of isolation resistors

is advantageous because it is well known in the art that a tip-network component includes isolation resistor. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Schmid et al by adding isolation resistors to the network component as taught by Holcombe et al since it is well known in the art to have an isolation resistor with the network component.

Conclusion

8. Claims 20-21 are allowed over the prior art.

9. Claims 10-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: regarding claim 10, the primary reason for the allowance for the claim is due to a probe comprising, in combination with other limitations, a second PCB that is abutted perpendicularly to a first PCB, with an edge of the second PCB opposite a first edge being abutted to the first PCB. Since claims 11-19 depend from claim 10, they also have allowable subject matter.

Regarding claim 20, the primary reason for the allowance of the claim is due to a method for forming a probe comprises, in combination with other limitations, abutting a cut edge of a first PCB to a second PCB and electrically coupling a signal routes of a first PCB to signal routes of that second PCB, by means of a via cross-sections, so that the first PCB extends perpendicularly from the second PCB. Since claim 21 depends from claim 20, it also has allowable subject matter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on (517) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Patent Examiner
Art Unit 2829

JMH
April 6, 2005